IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/198,215, filed July 17, 2002, ~~pending~~ now U.S. Patent 6,699,743, issued March 2, 2004, which is a continuation of application Serial No. 09/641,067, filed August 17, 2000, now U.S. Patent 6,458,663, issued October 1, 2002.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Additionally, blanket hardening techniques cause difficultly in fabricating IC devices including gate oxides of varying thicknesses. Hardened oxide layers generally will not grow significantly during subsequent thermal oxidation processes. Therefore, to fabricate an IC device having gate oxides of various thicknesses using a blanket hardening process, the gate oxide layer must be formed such that, after hardening, the hardened gate oxide layer is as thick as the thickest desired gate oxide. The hardened gate oxide layer must then be selectively etched back to a desired thickness where P-channel or N-channel devices having thinner gate oxides are to be formed. Such a process is disadvantageous because it adds the cost and complication associated with one or more additional etch steps. Moreover, known etching processes are difficult to control where only minute amounts of material must be removed. Thus, as the thickness of state of the art gate oxides shrinks well below ~~70~~, 70 ′, the need to etch back a hardened gate oxide layer becomes increasingly problematic and can only serve as a source of error, decreasing fabrication throughput as well as device reliability.